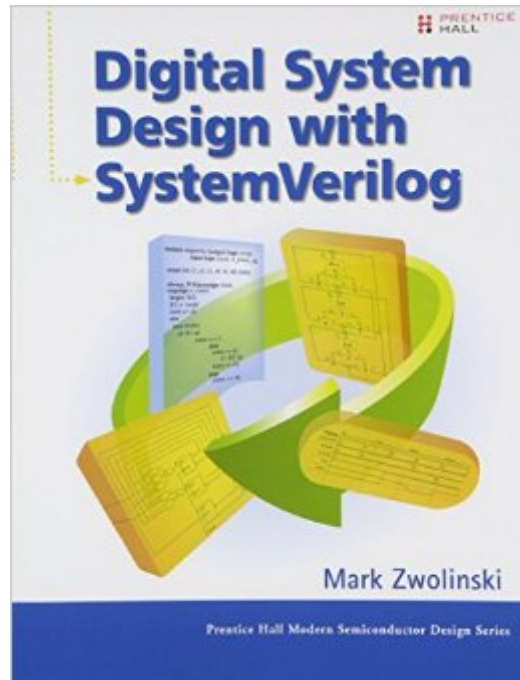


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# Digital System Design With SystemVerilog



## Synopsis

The Definitive, Up-to-Date Guide to Digital Design with SystemVerilog: Concepts, Techniques, and Code To design state-of-the-art digital hardware, engineers first specify functionality in a high-level Hardware Description Language (HDL) and today's most powerful, useful HDL is SystemVerilog, now an IEEE standard. Digital System Design with SystemVerilog is the first comprehensive introduction to both SystemVerilog and the contemporary digital hardware design techniques used with it. Building on the proven approach of his bestselling Digital System Design with VHDL, Mark Zwolinski covers everything engineers need to know to automate the entire design process with SystemVerilog from modeling through functional simulation, synthesis, timing simulation, and verification. Zwolinski teaches through about a hundred and fifty practical examples, each with carefully detailed syntax and enough in-depth information to enable rapid hardware design and verification. All examples are available for download from the book's companion Web site, [zwolinski.org](http://zwolinski.org). Coverage includes Using electronic design automation tools with programmable logic and ASIC technologies Essential principles of Boolean algebra and combinational logic design, with discussions of timing and hazards Core modeling techniques: combinational building blocks, buffers, decoders, encoders, multiplexers, adders, and parity checkers Sequential building blocks: latches, flip-flops, registers, counters, memory, and sequential multipliers Designing finite state machines: from ASM chart to D flip-flops, next state, and output logic Modeling interfaces and packages with SystemVerilog Designing testbenches: architecture, constrained random test generation, and assertion-based verification Describing RTL and FPGA synthesis models Understanding and implementing Design-for-Test Exploring anomalous behavior in asynchronous sequential circuits Performing Verilog-AMS and mixed-signal modeling Whatever your experience with digital design, older versions of Verilog, or VHDL, this book will help you discover SystemVerilog's full power and use it to the fullest.

## Book Information

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## Customer Reviews

This book may not be a comprehensive on systemVerilog Syntax. But if you know everything in this book, you will pass most of the Engineering interviews (everything in logic design, and validation) as it covers everything that you must know to start your career as an engineer. I had over 20 interviews with Intel's various groups and I wish I had this book earlier. Almost all of the questions, you can answer from this book. I really recommend this book if you are a computer engineer. The coeds in the book is in systemVerilog (like adders, dff, basic cpu, ...), if you know a bit of Verilog you are good to go. The following book is a better comprehensive book in systemVerilog if you need to learn s.v. from scratch: "SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling by Stuart Sutherland"

I don't know why this book don't have reviews. Before buying it I erroneously thought this lack of reviews was a good sign. Bad luck for me I spent so much!!!. This book is almost as brief as an abstract. I don't understand how a newbie could get some insight from it. I don't see any use for this book. Maybe those who already knows SystemVerilog and need a fast refreshing reading before getting involved into a project will be grateful. But for the rest of us who want to LEARN SV this is too far from the way to go.

I should have looked more closely at the contents. The books is perfect as an introduction, but I was looking for a deeper treatment.

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